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 Electron Devices, IEEE Transactions on
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 AbstractPlus References Full Text: PDF(304 KB) IEEE JNL</p> |
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 Monfray, S.; Souifi, A.; Boeuf, F.; Ortolland, C.; Poncet, A.; Militaru, L.; Chanemougam, T.;
 Nanotechnology, IEEE Transactions on
 Volume 2, Issue 4, Dec. 2003 Page(s):295 - 300
 AbstractPlus References Full Text: PDF(1035 KB) IEEE JNL</p> |
| <input type="checkbox"/> | <p>3. Dielectric pockets-a new concept of the junctions for deca-nanometric CMOS de
 Jurczak, M.; Skotnicki, T.; Gwoziecki, R.; Paoli, M.; Tormen, B.; Ribot, P.; Dutartre, D.; Galvier, J.;
 Electron Devices, IEEE Transactions on
 Volume 48, Issue 8, Aug. 2001 Page(s):1770 - 1775
 AbstractPlus References Full Text: PDF(152 KB) IEEE JNL</p> |
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 Jurczak, M.; Skotnicki, T.; Paoli, M.; Tormen, B.; Martins, J.; Regolini, J.L.; Dutartre, D. Lenoble, D.; Pantel, R.; Monfray, S.;
 Electron Devices, IEEE Transactions on
 Volume 47, Issue 11, Nov. 2000 Page(s):2179 - 2187
 AbstractPlus References Full Text: PDF(212 KB) IEEE JNL</p> |
| <input type="checkbox"/> | <p>5. Impact of the tunnel etching process on electrical performances of SON devices.
 Borel, S.; Arvei, C.; Bilde, J.; Caubet, V.; Chanemougame, D.; Monfray, S.; Ranica, R.;
 Microprocesses and Nanotechnology Conference, 2004. Digest of Papers. 2004 Intern
 Oct. 27-29, 2004 Page(s):50 - 51
 AbstractPlus Full Text: PDF(108 KB) IEEE CNF</p> |
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 Coronel, P.; Harrison, S.; Cerutti, R.; Monfray, S.; Skotnicki, S.;
 Integrated Circuit Design and Technology, 2004. ICICDT '04. International Conference</p> |

2004 Page(s):81 - 89

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7. **SON (silicon-on-nothing) technological CMOS platform: highly performant device cells**
Monfray, S.; Chanemougame, D.; Borel, S.; Talbot, A.; Leverd, F.; Planes, N.; Delille, I.; Palla, R.; Morand, Y.; Descombes, S.; Samson, M.-P.; Vulliet, N.; Sparks, T.; Vandoore, T.;
Electron Devices Meeting, 2004. IEDM Technical Digest. IEEE International
13-15 Dec. 2004 Page(s):635 - 638
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8. **First 80 nm SON (Silicon-On-Nothing) MOSFETs with perfect morphology and high performance**
Monfray, S.; Skotnicki, T.; Morand, Y.; Descombes, S.; Paoli, M.; Ribot, P.; Talbot, A.; Leverd, F.; Lefriec, Y.; Pantel, R.; Haond, M.; Renaud, D.; Nier, M.-E.; Vizios, C.; Louis, D.;
Electron Devices Meeting, 2001. IEDM Technical Digest. International
2-5 Dec. 2001 Page(s):29.7.1 - 29.7.4
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9. **16 nm planar NMOSFET manufacturable within state-of-the-art CMOS process technology: design and optimisation**
Boeuf, F.; Skotnicki, T.; Monfray, S.; Julien, C.; Dutartre, D.; Martins, J.; Mazoyer, P.; Ribot, P.; Sondergard, E.; Sanquer, A.;
Electron Devices Meeting, 2001. IEDM Technical Digest. International
2-5 Dec. 2001 Page(s):29.5.1 - 29.5.4
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Monfray, S.; Skotnicki, T.; Tavel, B.; Morand, Y.; Descombes, S.; Talbot, A.; Dutartre, D.; Mazoyer, P.; Palla, R.; Leverd, F.; Lefriec, Y.; Pantel, R.; Haond, M.; Charbuillet, C.; Buffet, N.;
Electron Devices Meeting, 2002. IEDM '02. Digest. International
8-11 Dec. 2002 Page(s):263 - 266
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11. **Highly-performant 38 nm SON (silicon-on-nothing) P-MOSFETs with 9 nm-thick channel**
Monfray, S.; Skotnicki, T.; Morand, Y.; Descombes, S.; Talbot, A.; Dutartre, D.; Leverd, F.; Palla, R.; Pantel, R.; Haond, M.; Nier, M.-E.; Vizios, C.; Louis, D.;
SOI Conference, IEEE International 2002
7-10 Oct. 2002 Page(s):20 - 22
[AbstractPlus](#) | Full Text: [PDF\(320 KB\)](#) IEEE CNF
12. **50 nm-Gate All Around (GAA)-Silicon On Nothing (SON)-devices: a simple way to integrate of GAA transistors within bulk MOSFET process**
Monfray, S.; Skotnicki, T.; Morand, Y.; Descombes, S.; Coronel, P.; Mazoyer, P.; Harrison, S.; Talbot, A.; Dutartre, D.; Haond, M.; Palla, R.; Lefriec, Y.; Leverd, F.; Nier, M.-E.; Vizios, C.;
VLSI Technology, 2002. Digest of Technical Papers. 2002 Symposium on
11-13 June 2002 Page(s):108 - 109
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13. **Highly performant double gate MOSFET realized with SON process**
Harrison, S.; Coronel, P.; Leverd, F.; Cerutti, R.; Palla, R.; Delille, D.; Borel, S.; Jullian, S.; Descombes, S.; Dutartre, D.; Morand, Y.; Samson, M.P.; Lenoble, D.; Talbot, A.; Villard, S.; Mazoyer, P.; Bustos, J.; Brut, H.; Cros, A.; Munteanu, D.; Autran, J.-L.; Skotnicki, T.;
Electron Devices Meeting, 2003. IEDM '03 Technical Digest. IEEE International
8-10 Dec. 2003 Page(s):18.6.1 - 18.6.4

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Fenouillet-Beranger, C.; Skotnicki, T.; Monfray, S.; Carriere, N.; Boeuf, F.;
SOI Conference, 2003. IEEE International
29 Sept.-2 Oct. 2003 Page(s):145 - 146
[AbstractPlus](#) | Full Text: [PDF\(296 KB\)](#) IEEE CNF
- ☐ **15. Short channel and back-gate coupling effects in silicon-on-nothing (SON) MOSFI**
Pretet, J.; Cristoloveanu, S.; Skotnicki, T.; Monfray, S.;
SOI Conference, 2003. IEEE International
29 Sept.-2 Oct. 2003 Page(s):122 - 123
[AbstractPlus](#) | Full Text: [PDF\(219 KB\)](#) IEEE CNF
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Chanemougame, D.; Poncet, A.; Monfray, S.; Souifi, A.; Bourdon, H.; Talbot, A.; Lever
Skotnicki, T.;
SOI Conference, 2004. Proceedings. 2004 IEEE International
4-7 Oct. 2004 Page(s):77 - 78
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- 